

Appl. No. 10/716,309
Amdt. dated November 20, 2006
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group 2825

PATENT

REMARKS/ARGUMENTS

Claims 1-29 are currently pending in the present office action. No new matter has been added.

In summary of the present office action, the Examiner has rejected claims 1-29 under 35 U.S.C. §103(a).

I. Rejection of claims 1-29 under 35 U.S.C. §103(a).

The Examiner has rejected claims 1-26 under 35 U.S.C. §103(a) as being unpatentable over DiGiacomo et al., U.S. Patent No. 4,630,219 ("DiGiacomo"). The Applicants respectfully submit that DiGiacomo does not disclose or suggest all of the elements of the cited claims. For example, claim 1, as amended, recites in part:

removing a first one of the abstract blocks from the logic block in response to placement information that indicates a design goal would be improved by rearranging at least a portion of the user design; and

placing the first abstract block into a different logic block on the programmable integrated circuit, wherein the functional attribute of removed abstract block corresponds with a functional attribute of the different logic block.

The Applicants respectfully submit that DiGiacomo does not disclose or suggest at least these elements of claim 1.

DiGiacomo discloses a method for "optimally assigning a plurality of different size elements to element positions in an array of element positions." (Col. 1:6-9). To this end, DiGiacomo discloses that the components are first "clustered and reordered." (Fig. 2; Col. 7:9-16).

Following the initial clustering and reordering, DiGiacomo determines a placement of the components in three phases (Fig. 2). The first placement phase is a unit size placement (Fig. 2:23), in which "all of the elements are treated as if they are the same size (defined as unit size), and optimum placement for the unit size placement is determined." (Col.

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2:44-47). The second placement phase (Fig. 2:24) of DiGiacomo replaces the unit size elements with "macro size elements, which bear rough approximations to the actual element sizes." (Col. 2:50-53). "For macro modeling, each component's size is roughly proportional to its actual size" (Col. 3:33-35). Finally, in a third placement phase (Fig. 2:25), "the optimally placed macro size elements are replaced by actual size elements, and placement is again optimized to take the exact sizes into account." (Col. 2:55-57).

With regard to "removing a first one of the abstract blocks from the logic block" in claim 1, the Examiner cites Col. 9:43-59. However, DiGiacomo states "the smaller components are removed and the unit size model is generated. The smaller components are removed from processing in the unit and macro modelling steps. This is done to simplify the overall placement problem and to remove insignificant placement problems during initial optimization in order to generate a relational placement based on connectivity of larger components." (Col. 9: 32-42). During the third placement phase, "the net list is updated to bring in any smaller components removed earlier." (Col. 37:3-5).

Thus, DiGiacomo removes small components during the first and second placement phases to simplify the placement problem. The first and second placement phases of DiGiacomo determine the placement of the remaining larger components. These removed components are then restored during the third placement phase, when placement is almost complete.

In contrast, claim 1 recites "removing a first one of the abstract blocks from the logic block in response to placement information that indicates a design goal would be improved by rearranging at least a portion of the user design." Unlike DiGiacomo, claim 1 does not remove abstract blocks from logic blocks based upon their size. Moreover, claim 1 does not remove abstract blocks from logic blocks so that fewer, larger blocks are considered during placement. Instead, claim 1 calls for removing an abstract block from a logic block based on placement information, rather than its size, and does this to improve a design goal, not to simplify placement of the remaining abstract blocks.

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Additionally, claim 1 recites "placing the first abstract block into a different logic block." Thus, claim 1 places the abstract block removed from one logic block into a different logic block. In contrast, DiGiacomo does not move small components from one cluster to another cluster. Instead, DiGiacomo removes small components from the design, performs a placement of the remaining components of the design, and then restores the small components and determines their placement.

Therefore, the Applicants respectfully submit that claim 1 and its dependents are patentable over DiGiacomo.

Claim 14 recites elements similar to claim 1. Applicants respectfully submit that claim 14 and its dependents are patentable over DiGiacomo for similar reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are patentable and in condition for allowance.

The Applicants invite the Examiner to telephone the undersigned if the Examiner believes a telephone conference would expedite prosecution of this application..

Respectfully submitted,



Jonathan M. Hollander
Reg. No. 48,717

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
Attachments
JMH:asb
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